OIPE IAP25
SEP 21 2006
PATENT & TRADEMARK OFFICE

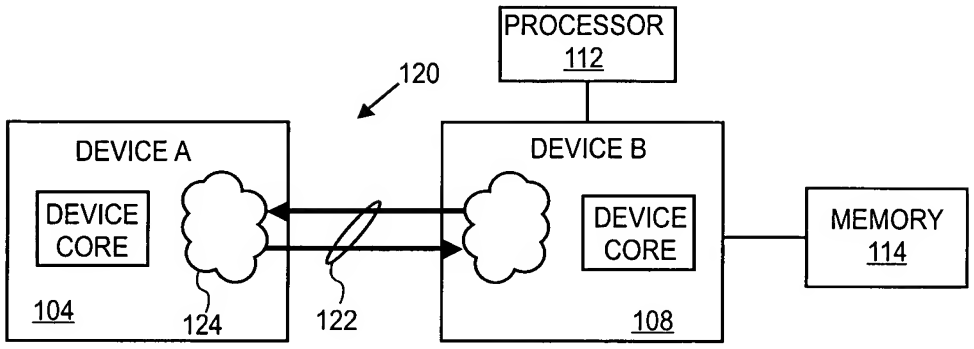


FIG. 1

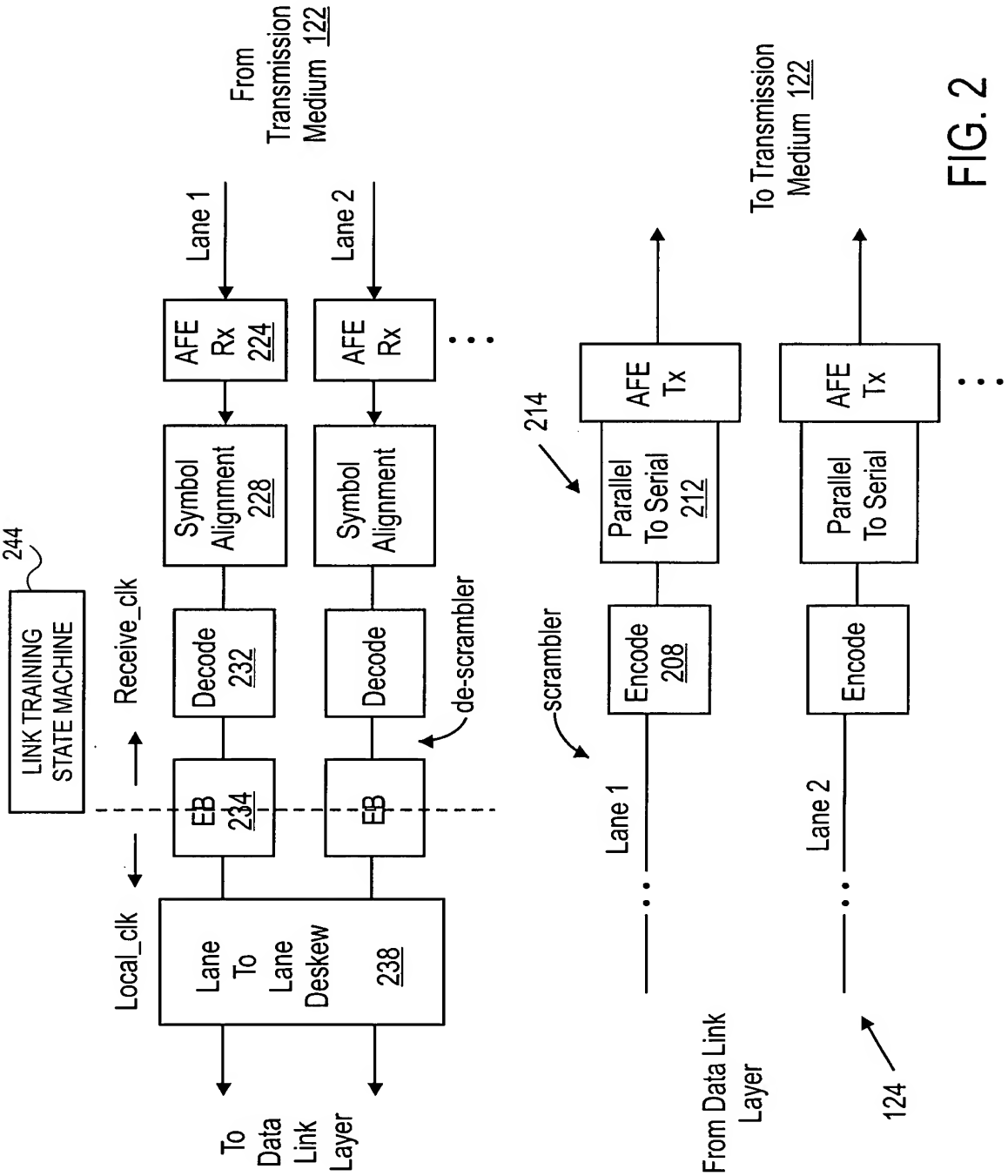

From Transmission Medium 122
Lane 1
Lane 2
AFE Rx 224
AFE Rx
Symbol Alignment 228
Symbol Alignment
Decode 232
Decode
EB 234
EB
244
LINK TRAINING STATE MACHINE
Receive_clk
de-scrambler
Local_clk
Lane To Lane Deskew 238
To Data Link Layer
214
Parallel To Serial 212
Parallel To Serial
Encode 208
Encode
scrambler
AFE Tx
AFE Tx
To Transmission Medium 122
Lane 1
Lane 2
From Data Link Layer
124

FIG. 2

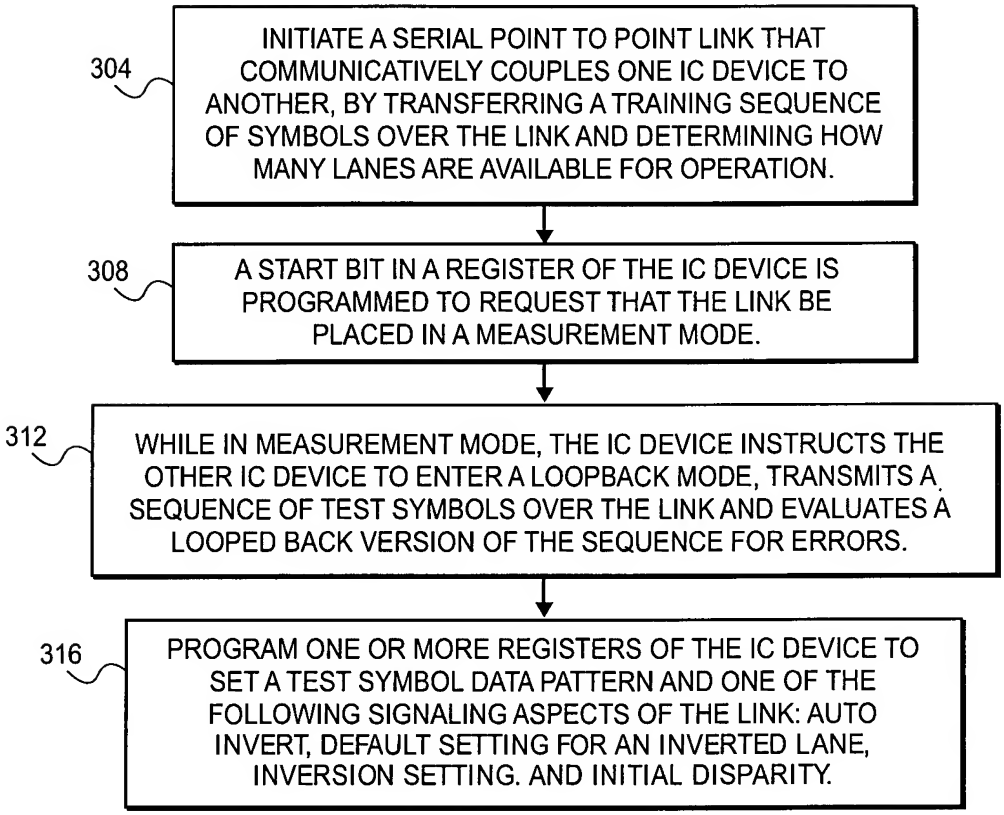

304
INITIATE A SERIAL POINT TO POINT LINK THAT COMMUNICATIVELY COUPLES ONE IC DEVICE TO ANOTHER, BY TRANSFERRING A TRAINING SEQUENCE OF SYMBOLS OVER THE LINK AND DETERMINING HOW MANY LANES ARE AVAILABLE FOR OPERATION.
308
A START BIT IN A REGISTER OF THE IC DEVICE IS PROGRAMMED TO REQUEST THAT THE LINK BE PLACED IN A MEASUREMENT MODE.
312
WHILE IN MEASUREMENT MODE, THE IC DEVICE INSTRUCTS THE OTHER IC DEVICE TO ENTER A LOOPBACK MODE, TRANSMITS A SEQUENCE OF TEST SYMBOLS OVER THE LINK AND EVALUATES A LOOPED BACK VERSION OF THE SEQUENCE FOR ERRORS.
316
PROGRAM ONE OR MORE REGISTERS OF THE IC DEVICE TO SET A TEST SYMBOL DATA PATTERN AND ONE OF THE FOLLOWING SIGNALING ASPECTS OF THE LINK: AUTO INVERT, DEFAULT SETTING FOR AN INVERTED LANE, INVERSION SETTING. AND INITIAL DISPARITY.

FIG. 3

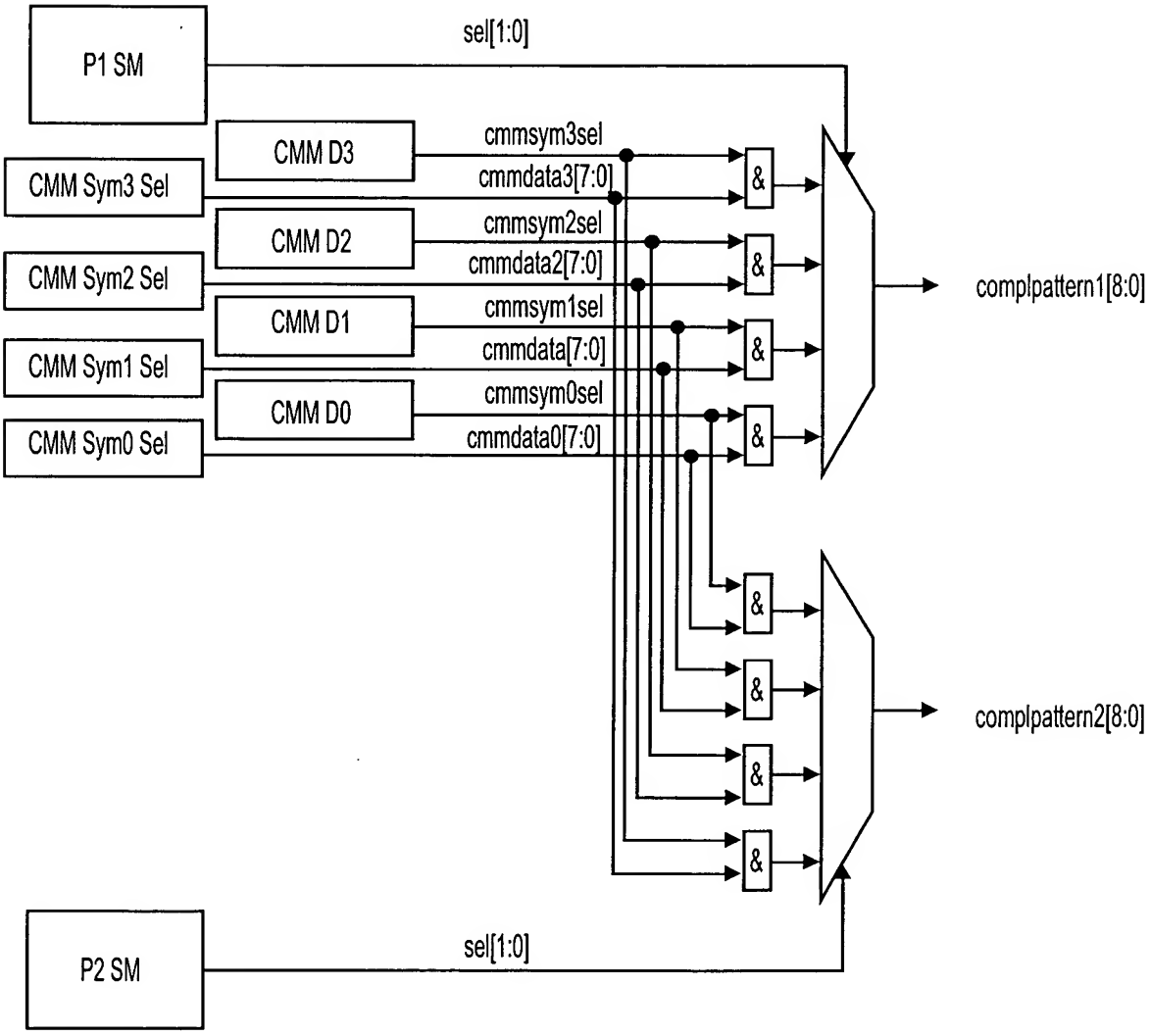

P1 SM
sel[1:0]
CMM D3
cmmsym3sel
CMM Sym3 Sel
cmmdata3[7:0]
CMM D2
cmmsym2sel
CMM Sym2 Sel
cmmdata2[7:0]
CMM D1
cmmsym1sel
CMM Sym1 Sel
cmmdata[7:0]
CMM D0
cmmsym0sel
CMM Sym0 Sel
cmmdata0[7:0]
&
complpattern1[8:0]
complpattern2[8:0]
P2 SM
sel[1:0]

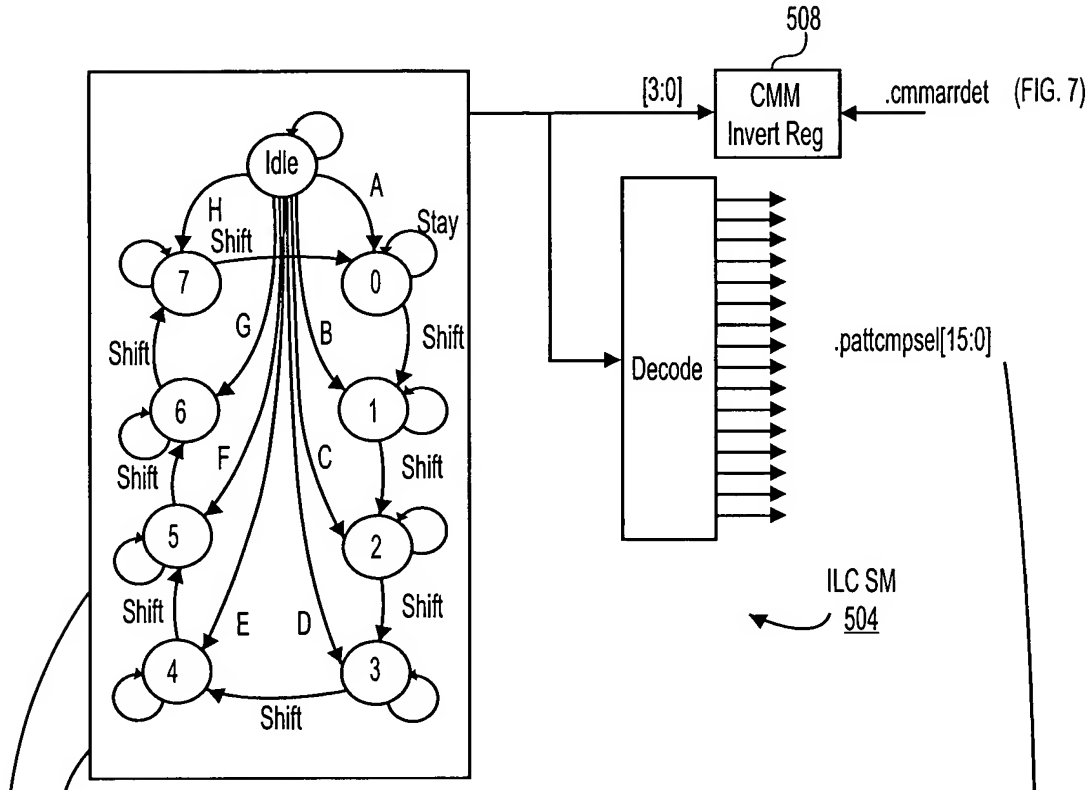
FIG. 4A

Register	D0	D1	D2	D3	D0	D1
Symbol	K28.5	D21.5	K28.5	D10.2	K28.5	D21.5
Disparity	0	1	1	0	0	1
Pattern	0011111010	1010101010	1100000101	0101010101	0011111010	1010101010

FIG. 4B

Register	D0	D0	D1	D2	D3	D0	D0
Symbol	K28.5	K28.5	D21.5	K28.5	D10.2	K28.5	K28.5
Disparity	0	1	0	1	1	0	1
Pattern	0011111010	1100000101	0011111010	1010101010	1100000101	0101010101	0011111010	1100000101

FIG. 4C



Shift : CMM Auto Invert = 1
Stay : CMM Auto Invert = 0

A: CMM Invert Enable	And CMM Invert Lane Number	=000
B: CMM Invert Enable	And CMM Invert Lane Number	=001
C: CMM Invert Enable	And CMM Invert Lane Number	=010
D: CMM Invert Enable	And CMM Invert Lane Number	=011
E: CMM Invert Enable	And CMM Invert Lane Number	=100
F: CMM Invert Enable	And CMM Invert Lane Number	=101
G: CMM Invert Enable	And CMM Invert Lane Number	=110
H: CMM Invert Enable	And CMM Invert Lane Number	=111

State	pattcmpse[0:15] 0 15
Idle	0000000000000000
0	1000000010000000
1	0100000001000000
2	0010000000100000
3	0001000000010000
4	0000100000001000
5	0000010000000100
6	0000001000000010
7	0000000100000001

FIG. 5

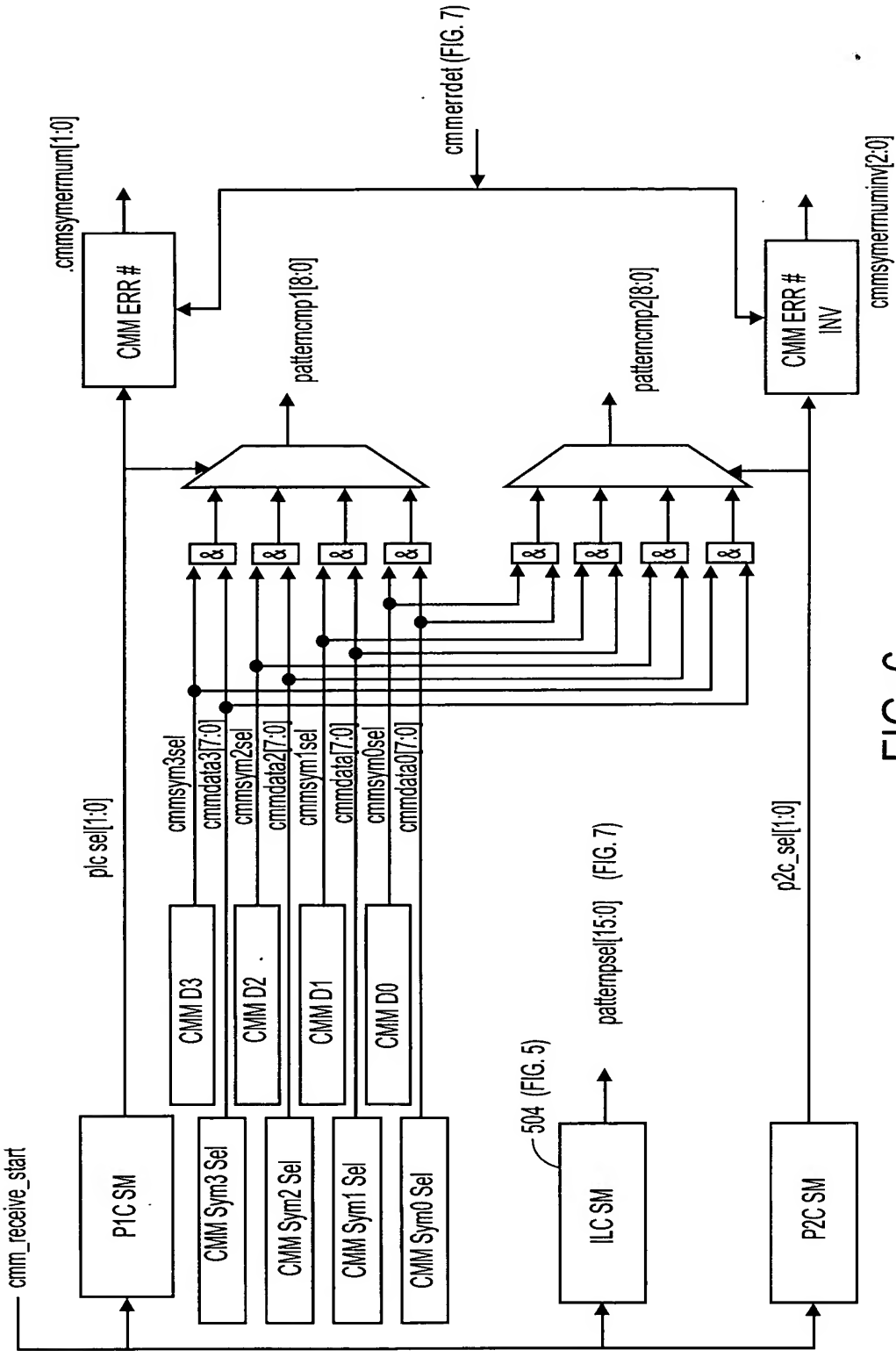

cmmerrdet (FIG. 7)
.cmmsymermum[1:0]
CMM ERR #
patterncmp1[8:0]
patterncmp2[8:0]
CMM ERR # INV
cmmsymermuminv[2:0]
&
cmmsym3sel
cmmdata3[7:0]
cmmsym2sel
cmmdata2[7:0]
cmmsym1sel
cmmdata1[7:0]
cmmsym0sel
cmmdata0[7:0]
p1c sel[1:0]
p2c_sel[1:0]
CMM D3
CMM D2
CMM D1
CMM D0
patternpsel[15:0] (FIG. 7)
504 (FIG. 5)
cmm_receive_start
P1C SM
CMM Sym3 Sel
CMM Sym2 Sel
CMM Sym1 Sel
CMM Sym0 Sel
ILC SM
P2C SM

FIG. 6

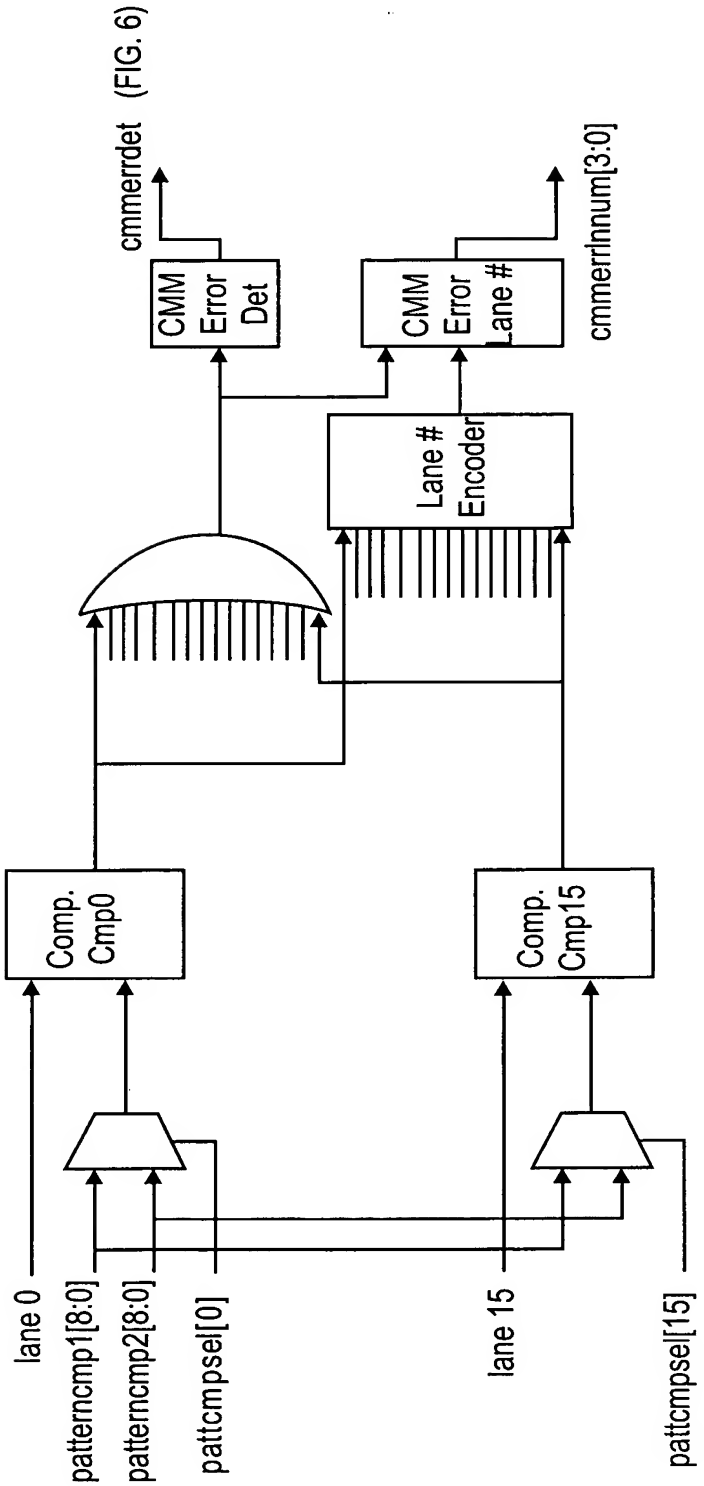

cmmerrdet (FIG. 6)
CMM Error Det
CMM Error Lane #
cmmerrlnnum[3:0]
Lane # Encoder
Comp. Cmp0
Comp. Cmp15
lane 0
patterncmp1[8:0]
patterncmp2[8:0]
pattcmpsel[0]
lane 15
pattcmpsel[15]

FIG. 7

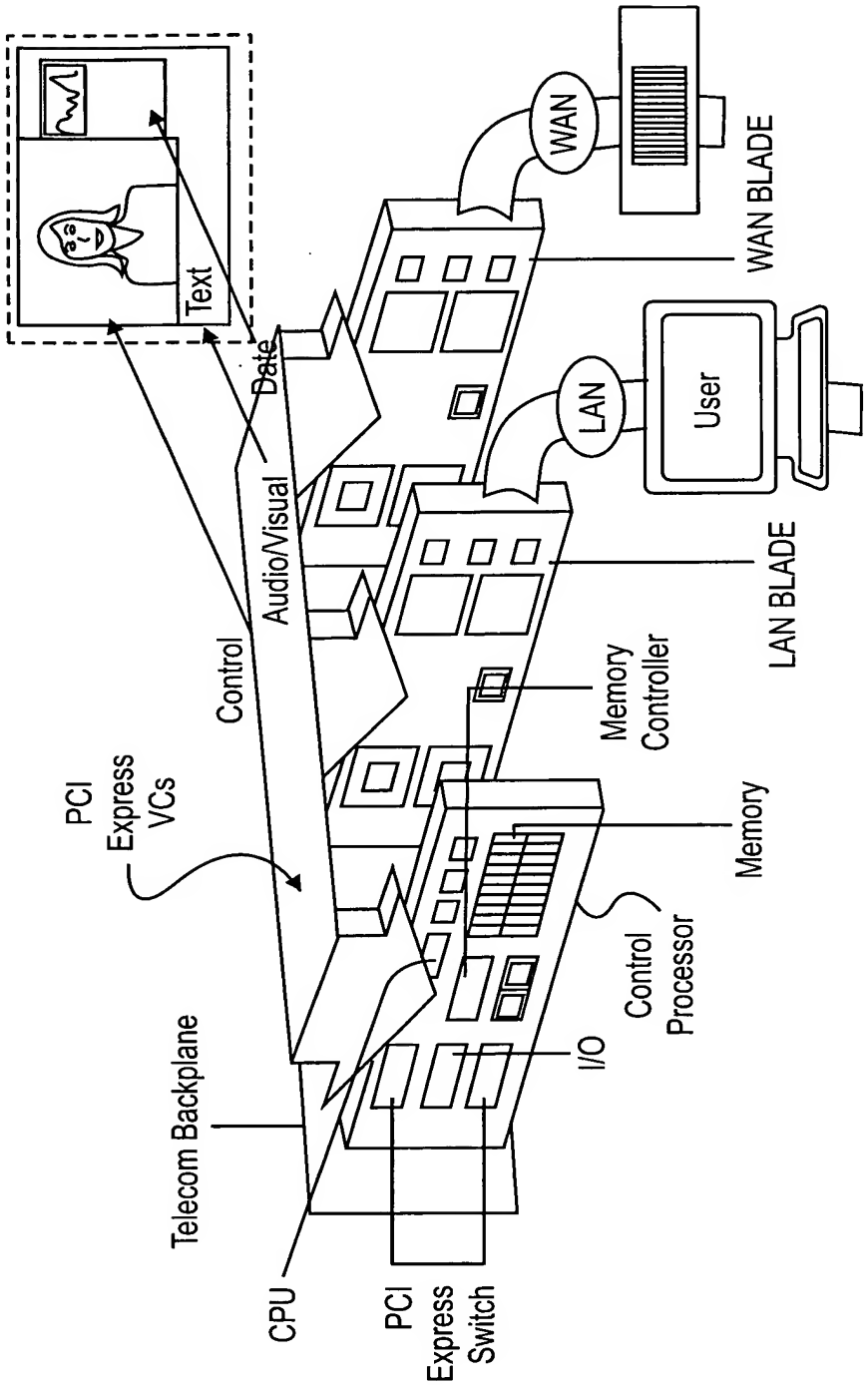

Text
Date
Audio/Visual
Control
PCI Express VCs
Telecom Backplane
CPU
PCI Express Switch
WAN
WAN BLADE
LAN
User
LAN BLADE
Memory Controller
Memory
Control Processor
I/O

FIG. 8

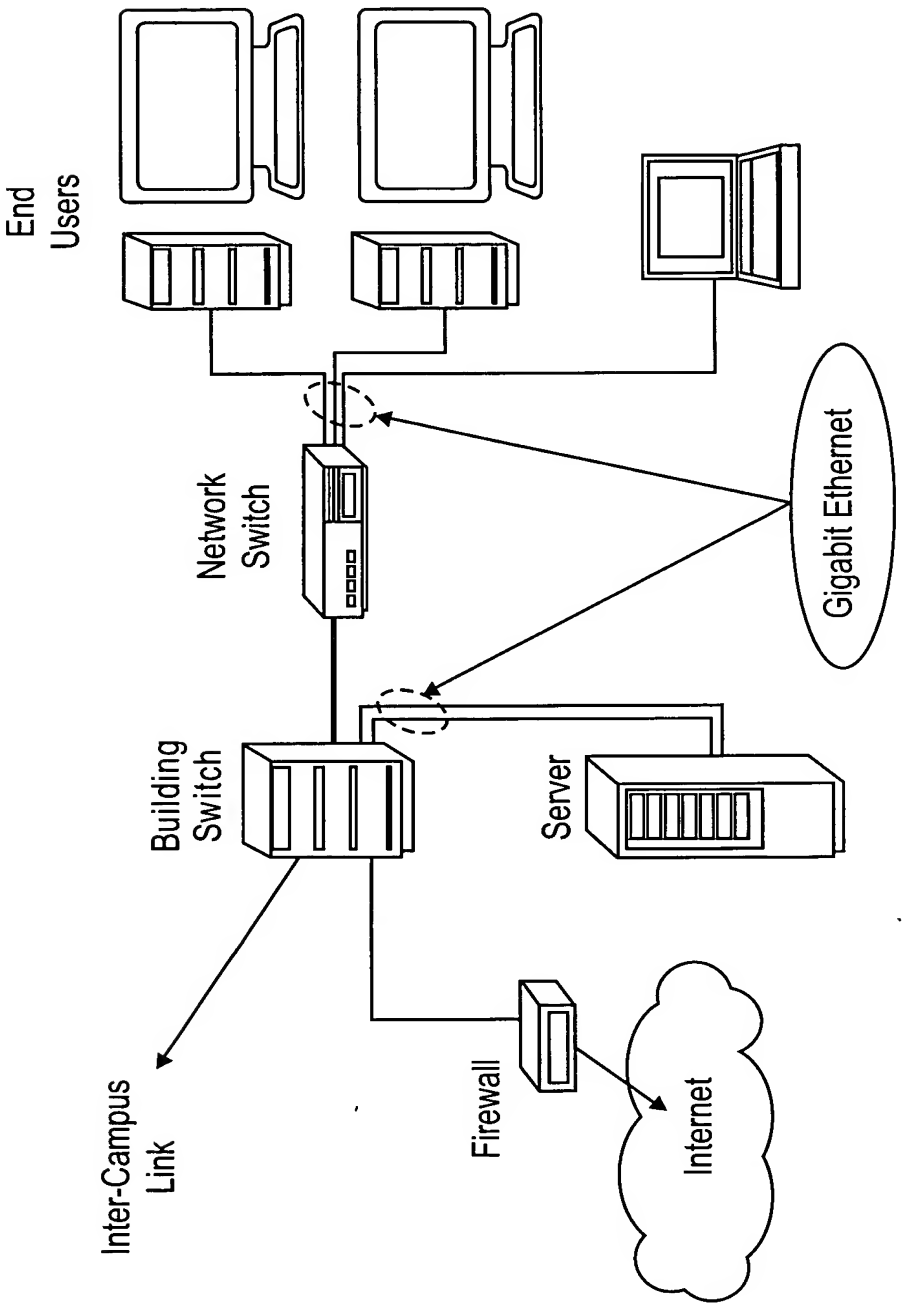

End Users
Network Switch
Gigabit Ethernet
Building Switch
Server
Inter-Campus Link
Firewall
Internet

FIG. 9